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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/316,699	05/21/1999	WILLIAM J. DALLY	AVI99-01	8189

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EXAMINER
LY, ANH VU H

ART UNIT	PAPER NUMBER
2667	13

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/316,699	DALLY ET AL.	
	Examiner	Art Unit	
	Anh-Vu H Ly	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 30-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 30-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This communication is in response to applicant's amendment filed on May 20, 2003. The proposed amendment to the claims has been entered. Claims 1-28 and 30-49 are pending.

Claim Objections

2. Claims 14 and 38 are objected to because of the following informalities:

With respect to claims 14 and 38, "A router as claimed in claim 1 in a network switch or router" recited in line 1 of claim 14 and "A network as claimed in claim 31 in a network switch or router" recited in line 1 of claim 38 are unclear. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-28 and 30-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Michael et al (EP O 886 454 A2) in view of Brant et al (US Patent No. 5,805,787). Hereinafter, referred to as Ben-Michael and Brant.

With respect to claims 1, 16, 31, and 40, Ben-Michael discloses (page 5, line 20 – page 6, line 33; page 7, line 41-42 and Fig. 7) a block diagram illustrating on-chip memory and off-chip memory for storing data packets (information units) or credits in a network switch or router; Wherein, on-chip memory allows rapid access for reading and writing (a first set of rapidly accessible buffers which store information units received at an input link) and wherein, off-chip

memory involves a delay in accessing and processing data packets or credits (a second set of buffers for the information units that are accessed more slowly than the first set).

Ben-Michael does not disclose the first set of buffers operating as a cache with information units being evicted to the second set of buffers according to an algorithm other than order of receipt in the first buffer.

Brant discloses (col. 8 lines 50-54) that logical data within the table entry can be evicted in a random, revolving, least recently used or fastest fit algorithm. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include an eviction algorithm such as least recently used or fastest fit algorithm in Ben-Michael's system, as suggested by Brant, to efficiently manage the information units.

With respect to claims 2, 17, and 32, Ben-Michael discloses in Fig. 1, ATM switches E and F are connected via interface 32 and 34 for directing traffic between among stations A-D. Therefore, "router processing is implemented on one or more router IC chips" recited in line 2 is inherent to Ben-Michael in accordance to Fig. 1. Ben-Michael discloses in Fig. 7, on-chip memory 710 is resided on the router IC chips (first set of buffers is located on the router IC chips); wherein, off-chip memory 723 is separated resided from the router IC chips (second set of buffers is located on memory chips separate from the router IC chips).

With respect to claims 3, 18, 33, and 41, Ben-Michael discloses in Fig. 1, ATM switches E and F are connected via interface 32 and 34 for directing traffic between a plurality of stations A-D, wherein, data packets are transmitted over the virtual circuits. Further, Ben-Michael

discloses (see Abstract) that the off-chip memory can be used to store data packets when the on-chip portion of the FIFO is full. This means, the off-chip memory can store packets of a number of virtual channels (second set of buffers holds information units for a complete set of virtual channels).

With respect to claims 4, 19, 34, and 42, Ben-Michael discloses (page 5, line 41-43 and Fig. 7) that the on-chip memory is a SRAM (a buffer pool) wherein SRAM is divided into four consecutive parts to form the logical banks. Each one of the four physical parts is actually a small FIFO with a read and write pointer (a pointer array of pointers to buffered information units).

With respect to claims 5, 7, 20, 22, 35, and 43, Ben-Michael discloses a method and apparatus for expanding on-chip FIFO into local memory. Ben-Michael does not disclose first set of buffers is organized as a set-associative cache. Brant discloses (col. 8, lines 42-49) a set associative strategy employed in a disk based disk cache, wherein, the set association uses a simple function like a modulo operation to map a logical block address to a table entry. Each table entry contains a fixed number of physical locations in which the logical block might be located. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include such set associative strategy in Ben-Michael's system, as suggested by Brant, to efficiently managed the stored packets.

With respect to claims 6 and 21, Ben-Michael discloses in Fig. 6, in the activate FIFO, each entry comprising two columns, first column identifying the virtual circuit number and the second column identifying the number of credits. However, Ben-Michael discloses (page 7, line 41-42) that the FIFO can be used to store data packets instead of credits. This implies that, the second column can store the data packets associated with such virtual circuit number (set associative cache contains a single information unit).

With respect to claims 8, 10, 23, 25, 36-37, and 44, the limitation "flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers" recited in lines 1-3 is inherent to Ben-Michael. Wherein, Ben-Michael discloses (col. 2, lines 10-11) that credit based flow control is used to control the amount of data transmitted by a source node so that there is always a buffer available in the destination node to hold the data. Further, Ben-Michael discloses (see Abstract) that data is transferred to the off-chip memory when the on-chip memory is full. This means, by employing the credit based flow control, the source will hold its data while the data packets stored on-chip memory is offloaded to the off-chip memory, since no credits are being returned upstream to notify the source that a buffer is available at the destination.

With respect to claims 9 and 24, Ben-Michael discloses (col. 2, lines 10-11) a method of employing credit based flow control in an ATM network. Ben-Michael does not disclose that the flow control is blocking. However, blocking method is known in the art for controlling the traffic between nodes. It would have been obvious to one having ordinary skill in the art at the

time the invention was made to include such blocking control method in Ben-Michael's system, for controlling data transmission between nodes in order to prevent an overflow in the network.

With respect to claims 11, 12, 26, and 27, Ben-Michael discloses (page 5, line 20 – page 6, line 33; page 7, line 41-42 and Fig. 7) a block diagram illustrating on-chip memory and off-chip memory for storing data packets (information units) or credits in a network switch or router; Wherein, on-chip memory allows rapid access for reading and writing (a first set of rapidly accessible buffers which store information units received at an input link) and wherein, off-chip memory involves a delay in accessing and processing data packets or credits (a second set of buffers for the information units that are accessed more slowly than the first set). Further, as illustrated in Fig. 7, FIFO bank 1 stores and holds data packs for transferring to the off-chip memory (miss status registers and eviction buffer to hold information units and entries waiting for access to the second set of buffers).

With respect to claims 13 and 28, Ben-Michael discloses in Fig. 1, ATM switches E and F are connected via interface 32 and 34 for directing traffic between a plurality of stations A-D, wherein, data packets are transmitted over the virtual circuits (a router is in a multi-computer interconnection network).

With respect to claims 14 and 38, as best understood, ATM switches E and F as shown in Fig. 1 are network switches (a router is a network switch).

With respect to claims 15, 30, 39, and 45, ATM switches E and F are connected via interface 32 and 34 for directing traffic between a plurality of stations A-D, wherein, data packets or cells (flits) are transmitted over the virtual circuits (the router is a fabric router and information units are flits).

With respect to claims 46-49, Ben-Michael discloses in Fig. 7, on-chip memory (first set of rapidly accessible buffers) is shared (dynamically assignable) by all of the virtual channels for storing data packets (buffers of first set of rapidly accessible buffers are dynamically assignable to virtual channels to serve as a virtual channel buffer cache).

Response to Arguments

4. Applicant's arguments with respect to claims 1-28 and 30-49 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 703-306-5675. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703-305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

avl
July 30, 2003

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 7/31/03